AMENDMENTS TO THE CLAIMS

Pursuant to 37 C.F.R. § 1.121 the following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented): A semiconductor device, comprising:

a semiconductor element with an area for a main surface of 1 mm^2 or greater;

a substrate having a thermal conductivity of 170 W/m-K or greater and having an upper surface on which said element is mounted and a bottom surface which is positioned on the opposite side; and

a ratio H/L being greater than or equal to 0.3 but less than 1.25, with L being the length in the long direction of a main surface of said semiconductor element, and H being the distance from a semiconductor element mounting part on said upper surface of said substrate to said bottom surface.

2-3. (Cancelled)

4. (Previously Presented) The semiconductor device according to claim 1, further comprising:

a ratio of Y/L being equal to or greater than 2, with Y being the distance from one end of the bottom surface of the substrate to the opposite end of the bottom surface of the substrate along the same plane as L.

5. (Previously Presented) The semiconductor device according to claim 1, wherein the thermal conductivity of the substrate is equal to or greater than 200 W/m-K.

6. (Previously Presented) The semiconductor device according to claim 1, wherein the ratio H/L is greater than 0.45 but less than 1.25.

7. (Previously Presented) The semiconductor device according to claim 1, wherein the distance H is greater than or equal to 0.3 mm but less than or equal to 10 mm.

8. (Withdrawn): A semiconductor device, comprising:

a semiconductor element with an area for a main surface of 1 mm^2 or greater;

a substrate having a thermal conductivity of 170 W/m-K or greater and having an upper surface and a bottom surface which is positioned on the opposite side of the upper surface;

a cavity formed in the upper surface of the substrate, the semiconductor element being mounted within the cavity;

a ratio H/L being greater than 0.3 but less than 1.25, with L being the length in the long direction of a main surface of said semiconductor element, and H being the distance from a semiconductor element mounting within the cavity on the upper surface of the substrate to the bottom surface of the substrate.

9. (Withdrawn) The semiconductor device according to claim 8, further comprising:

a ratio of Y/L being equal to or greater than 2, with Y being the distance from one end of the bottom surface of the substrate to the opposite end of the bottom surface of the substrate along the same plane as L.

10. (Withdrawn) The semiconductor device according to claim 8, wherein the thermal conductivity of the substrate is equal to or greater than 200 W/m-K.

11. (Withdrawn) The semiconductor device according to claim 8, further comprising:

a metal layer formed on the upper surface of the substrate.

12. (Withdrawn) The semiconductor device according to claim 11, wherein a maximum roughness Rmax of the metal layer is in a range of 0.1 to 20 micrometers.

13. (Withdrawn) The semiconductor device according to claim 8, further comprising:

a hole formed in the substrate;

a pin disposed within the hole, the pin providing electrical power to the semiconductor element;

a bonding wire that electrically connects the pin to the semiconductor element; and

an insulating material which fills a space between the inner surface of the hole and the pin.

14. (Withdrawn) The semiconductor device according to claim 8, further comprising:

a connection member provided on the upper surface of the substrate;

an insulating plate provided on top of the connection member;

an electrode provided on top of the insulating plate;

an contact prevention member to prevent the connection member from contacting the cavity;

and

a bonding wire that electrically connects the electrode to the semiconductor element.

15. (Withdrawn) The semiconductor device according to claim 14, wherein the contact prevention member is a groove.

16. (Withdrawn) The semiconductor device according to claim 15, wherein a width of the groove is greater than or equal to 50 micrometers and less than 1 millimeter.

17. (Withdrawn) The semiconductor device according to claim 11, further comprising:

an intermediate layer provided between the upper surface of the substrate and the metal layer.

18. (Withdrawn) The semiconductor device according to claim 17, wherein the intermediate layer has a thickness between 0.01 micrometers and 5 micrometers.

19. (Previously Presented): A semiconductor device, comprising:

a semiconductor element with an area for a main surface of 1 mm^2 or greater;

a substrate having a thermal conductivity of 170 W/m-K or greater and having an upper surface on which the semiconductor element is mounted and a bottom surface which is positioned on the opposite side;

a metal layer formed on the upper surface of the substrate; and

a ratio H/L being greater than 0.3 but less than 1.25, with L being the length in the long direction of a main surface of said semiconductor element, and H being the distance from a semiconductor element mounting part on said upper surface of said substrate to said bottom surface.

20. (Previously Presented) The semiconductor device according to claim 19, wherein a maximum roughness Rmax of the metal layer is in a range of 0.1 to 20 micrometers.

21. (Previously Presented) The semiconductor device according to claim 19, further comprising:

a hole formed in the substrate;

a pin disposed within the hole that supplies power to the semiconductor element; and

an insulating material which fills a space between the inner surface of the hole and the pin.

22. (Previously Presented) The semiconductor device according to claim 19, further comprising:

a terminal plate that supplies power to the semiconductor element;

a connection member which connects between the substrate and the terminal plate.

23. (Withdrawn) A semiconductor device, comprising:

a semiconductor element with an area for a main surface of 1 mm^2 or greater;

a substrate having a thermal conductivity of 170 W/m-K or greater and having an upper surface on which said element is mounted and a bottom surface which is positioned on the opposite side;

a ratio H/L being greater than or equal to 0.3, with L being the length in the long direction of

a main surface of said semiconductor element, and H being the distance from a semiconductor element mounting part on said upper surface of said substrate to said bottom surface; and

a ratio H/Y being greater than or equal to 0.4, with Y being the distance from one end of the bottom surface of the substrate to the opposite end of the bottom surface of the substrate along the same plane as L.

24. (Withdrawn) The semiconductor device according to claim 23, wherein the H/Y ratio is greater than or equal to 0.4 but less than 0.67.

25. (Withdrawn) The semiconductor device according to claim 23, wherein during operation of the semiconductor element, the rate of temperature increase of the semiconductor device is less than 20%, thereby achieving effective heat dissipation of the semiconductor element.